IN THE CLAIMS

The current pending claims are as follows:

1. (Previously Presented) A system for populating parameters of design cells defining a physical layout of a hierarchical semiconductor structure comprising:

a global file of global geometric variables relating to a physical layout of element blocks of the hierarchical semiconductor structure;

a plurality of local files, each local file containing parameters relating a plurality of local variables to the global geometric variables; and,

a plurality of programmable design cells, each cell corresponding to a local file and having a set of parameters created by relating the corresponding local variables within a local file to appropriate global geometric variables from the global file such that changes of global geometric variables in the global file may cause changes in the design cells for the physical layout of the hierarchical semiconductor structure in accordance with parameters in the local files.

2. (Previously Presented) The system of claim 1, wherein at least one local file comprises an inherit file which inherits parameters from the global file.

3. (Previously Presented) The system of claim 1, wherein each local file comprises an instance file.

4. (Previously Presented) The system of claim 1, further comprising a plurality of master files, each master file acting as an initial version of a corresponding local file.

5. (Previously Presented) The system of claim 1, further comprising a cleansheet file containing current design rules for the plurality of cells such that values for the global variables of the global file are derived therefrom.

6. (Previously Presented) The system of claim 5, further comprising an extract mechanism to update values for the global variables of the global file from the current design rules of the cleansheet file.

7. (Previously Presented) The system of claim 1, further comprising a mechanism to display values for the local variables of a local file, and permit a user to change one or more of the values.

8. (Previously Presented) The system of claim 1, further comprising an update mechanism to update the set of parameters of each cell by reading values for the global variables to which the local variables of the corresponding local file correspond.

9. (Previously Presented) A computer-readable medium having a computer program stored thereon to cause a suitably equipped computer to update a set of geometric parameters of a design cell defining a physical layout of a hierarchical semiconductor structure by relating local geometric variables of a local file for the design cell to a global file of global geometric variables relating to layout of element blocks of a hierarchical semiconductor structure such that changes of a global geometric variable in the global file may cause changes in the design cell for the physical layout of the hierarchical semiconductor structure in accordance with parameters in the local files.

10. (Original) The computer-readable medium of claim 9, wherein each local file comprises an inherit file.

11. (Original) The computer-readable medium of claim 9, wherein each local file comprises an instance file.

12. (Original) The computer-readable medium of claim 9, further having a second computer program stored thereon to cause the suitably equipped computer to update values for the global variables of the global file from current design rules of a cleansheet file.

13. (Original) The computer-readable medium of claim 9, further having a second computer program stored thereon to display values for the local variables of the local file, and permit a user to change one or more of the values.

14. (Original) The computer-readable medium of claim 9, wherein the computer program is written in the SKILL computer language that is utilized in conjunction with Design Framework II software available from Cadence Design Systems, Inc.

15. (Previously Presented) A computer comprising:

a processor;

a computer-readable medium;

a global file of global geometric variables stored on the medium, at least some of the global geometric variables relating to physical layout of element blocks of hierarchical semiconductor structures;

a plurality of local files stored on the medium, each local file containing parameters relating a plurality of local variables to the global geometric variables; and,

a computer program executed by the processor from the medium to automatically update a set of parameters for each of a plurality of programmable design cells for the physical layout of a hierarchical semiconductor structure, each cell having a corresponding local file, by reading, from the global file, values for the global geometric variables to which the local variables of the local file correspond.

16. (Original) The computer of claim 15, wherein each local file comprises an instance file.

17. (Original) The computer of claim 15, wherein each local file comprises an inherit file.

18. (Original) The computer of claim 15, further comprising a second computer program executed by the processor from the medium to display values for the local variables of a local file, and permit a user to change one or more of the values.

19. (Original) The computer of claim 15, further comprising a plurality of master files stored on the medium, each master file acting as an initial version of a corresponding local file.

20. (Original) The computer of claim 15, further comprising a cleansheet file stored on the medium and containing current design rules for the plurality of cells such that values for the global variables of the global file are derived therefrom.

21. (Original) The computer of claim 20, further comprising a second computer program executed by the processor from the medium to update values for the global variables of the global file from the current design rules of the cleansheet file.

22. (Previously Presented) A computerized method comprising:

changing within a cleansheet file at least one of a plurality of design rules for defining the physical layout of a hierarchical semiconductor structure;

updating values for a plurality of global geometric variables of a global file based on the design rules of the cleansheet file; and,

updating a set of parameters of a programmable design cell for the physical layout of the hierarchical semiconductor structure by relating corresponding local variables of a local file corresponding to the programmable design cell to corresponding global geometric variables of the global file.

23. (Original) The computerized method of claim 22, wherein each local file comprises an inherit file.

24. (Original) The computerized method of claim 22, wherein each local file comprises an instance file.

25. (Original) The computerized method of claim 22, wherein the computerized method is performed in conjunction with Design Framework II software available from Cadence Design Systems, Inc.

26. (Previously Presented) A system for populating parameters of design cells defining a physical layout of a hierarchical semiconductor structure comprising:

a global file of global geometric variables relating to a physical layout of element blocks of the hierarchical semiconductor structure;

an extract mechanism to update values for the global geometric variables of the global file;

a plurality of local files, each local file containing parameters relating a plurality of local variables to the global geometric variables;

a plurality of programmable design cells, each design cell corresponding to a local file and having a set of parameters;

an update mechanism to update the set of parameters of each design cell by relating values for the global geometric variables from the global file to which local variables of the corresponding local file correspond such that changes of global geometric variables in the global file may cause changes in the design cells for the physical layout of the hierarchical semiconductor structure in accordance with parameters in the local files;

27. (Previously Presented) The system of claim 26, wherein at least one local file comprises an inherit file which inherits parameters from the global file.

28. (Previously Presented) The system of claim 26, wherein each local file comprises an instance file.

29. (Previously Presented) The system of claim 26, wherein the system includes a computer having a display.

30. (Previously Presented) A computer-readable medium having a computer program stored thereon to cause a suitably equipped computer to update a set of geometric parameters of a design cell defining a physical layout of a hierarchical semiconductor structure for a memory device by relating local geometric variables of a local file for the design cell to a global file of global geometric variables relating to layout of element blocks of hierarchical semiconductor structures for the memory device such that changes of a global geometric variable in the global file may cause changes in the cells for the physical layout of the hierarchical semiconductor structure of the memory device in accordance with parameters in the local files.

31. (Previously Presented) The computer-readable medium of claim 30, further having a second computer program stored thereon to cause the suitably equipped computer to update values for the global variables of the global file from current design rules of a cleansheet file.

32. (Previously Presented) The computer-readable medium of claim 30, further having a second computer program stored thereon to display values for the local variables of the local file, and permit a user to change one or more of the values.

33. (Previously Presented) A computerized method comprising:

changing one or more design rules for defining the physical layout of a hierarchical semiconductor structure of a memory device;

updating values for a plurality of global geometric variables of a global file based on the changed design rules; and

updating a set of parameters of a programmable design cell for the physical layout of the hierarchical semiconductor structure of the memory device by relating corresponding local variables of a local file corresponding to the programmable design cell to corresponding global geometric variables of the global file.

34. (Previously Presented) The computerized method of claim 22, wherein changing design rules for defining the physical layout of a hierarchical semiconductor structure of a memory device includes changing the design rules within a cleansheet file.

35. (Previously Presented) The computerized method of claim 22, wherein each local file comprises an inherit file.

36. (Previously Presented) The computerized method of claim 22, wherein each local file comprises an instance file.